Claims

1. A digital true random number generator circuit, comprising a linear feedback shift register having an input and an output, a system clock having a system clock frequency value for driving said shift register, and a free running oscillator operatively connected to said input of said shift register, said generator circuit further comprising at least one further free running oscillator operatively connected to said input, said oscillators and said system clock having different oscillation frequency values, the greatest common divisor of which having the value one.

2. A digital true random number generator circuit according to claim 1, wherein each free-running oscillator is designed as a ring oscillator having a plurality of cascade connected inverter circuits in a sequence and an output.

3. A digital true random number generator circuit according to claim 2, wherein each ring oscillator has an odd number of inverter circuits.

4. A digital true random number generator circuit according to claim 2, wherein each ring oscillator has an odd number of inverter circuits and the number of inverter circuits of each ring oscillator differ by two.

5. A digital true random number generator circuit according to claim 2, wherein each ring oscillator is operatively connected to a separate input of an exclusive OR-circuit.

6. A digital true random number generator circuit according to claim 5, wherein said exclusive OR-circuit having an output which is operatively connected to an input of a latching circuit;

said system clock is operatively connected to a clock input of said latching circuit; and

said latching circuit having an output which is operatively

connected to the input of said linear feedback shift register, for driving said shift register.

7. A digital true random number generator circuit according to claim 6, wherein said latching circuit is a D-type flip flop.

8. A digital true random number generator circuit according to claim 1, wherein said linear feedback shift register has a plurality of n cascade connected delay stages, said stages being divided into a first sub-plurality of i stages having an output operatively connected as a first input to a further exclusive OR-circuit;

said output of said linear feedback shift register being operatively connected to an input of a NOR-circuit;

said NOR-circuit having an output which operatively connects to a second input of said further exclusive OR-circuit; and

said further OR-circuit having a third input which forms the input of said linear feedback shift register, for driving said register.

9. A digital true random number generator circuit according to claim 8, wherein i <= n.

10. An Application Specific Integrated Circuit (ASIC) comprising a digital true random number generator circuit, said generator circuit comprising a linear feedback shift register having an input and an output, a system clock having a system clock frequency value for driving said shift register, and a free running oscillator operatively connected to said input of said shift register, said generator circuit further comprising at least one further free running oscillator operatively connected to said input, said oscillators and said system clock having different oscillation frequency values, the greatest common divisor of which having the value one.

11. An encryption device comprising means for encrypting and provided with a digital true random number generator circuit, said generator circuit comprising a linear feedback shift register having an

input and an output, a system clock having a system clock frequency value for driving said shift register, and a free running oscillator operatively connected to said input of said shift register, said generator circuit further comprising at least one further free running oscillator operatively connected to said input, said oscillators and said system clock having different oscillation frequency values, the greatest common divisor of which having the value one.

12. A transactions terminal comprising means for performing transactions and provided with a digital true random number generator circuit, said generator circuit comprising a linear feedback shift register having an input and an output, a system clock having a system clock frequency value for driving said shift register, and a free running oscillator operatively connected to said input of said shift register, said generator circuit further comprising at least one further free running oscillator operatively connected to said input, said oscillators and said system clock having different oscillation frequency values, the greatest common divisor of which having the value one.